

DATA SHEET

TDA8775

**Triple 10-bit video Digital-to-Analog
Converter (DAC)**

Preliminary specification
File under Integrated Circuits, IC02

1996 Aug 14

Triple 10-bit video Digital-to-Analog Converter (DAC)

TDA8775

FEATURES

- 10-bit resolution
- Sampling rate up to:
 - 50 MHz for normal mode; $R_L = 37.5 \Omega$
 - 35 MHz for LOW power mode; $R_L = 150 \Omega$
- Internal current reference
- Current reference selector for:
 - normal mode, $R_L = 37.5 \Omega$ (typ.)
 - low-power mode, $R_L = 150 \Omega$ (typ.)
- No deglitching circuit required
- $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ control inputs
- 0.66 V output voltage range on red and blue channels
- 1 V output voltage range on green channel (including sync)
- $\overline{\text{BLANK}}$ control input on the 3 channels
- + 5 V power supply.

APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing.

GENERAL DESCRIPTION

The TDA8775 consists of three 10-bit video Digital-to-Analog Converters (DACs). They convert the digital input signals into current outputs at a maximum conversion rate of 50 MHz.

The DACs are based on current source architecture with selectable current reference.

The devices are fabricated in a 5 V CMOS process that ensures high functionality with low power dissipation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	SLT = 1; $R_L = 37.5 \Omega$	–	67	tbf	mA
		SLT = 0; $R_L = 150 \Omega$	–	16	tbf	mA
I_{DDD}	digital supply current	SLT = 1; $R_L = 37.5 \Omega$	–	15	tbf	mA
		SLT = 0; $R_L = 150 \Omega$	–	10	tbf	mA
INL	DC integral non-linearity		–	± 1	± 2	LSB
DNL	DC differential non-linearity		–	± 0.7	± 1.0	LSB
$f_{\text{clk(max)}}$	maximum clock frequency	SLT = 1; $R_L = 37.5 \Omega$	50	–	–	MHz
		SLT = 0; $R_L = 150 \Omega$	35	–	–	MHz
P_{tot}	total power dissipation	SLT = 1; $R_L = 37.5 \Omega$; $f_{\text{clk}} = 50 \text{ MHz}$	–	410	tbf	mW
		SLT = 0; $R_L = 150 \Omega$; $f_{\text{clk}} = 35 \text{ MHz}$	–	130	tbf	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8775G	LQFP48	plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4 \text{ mm}$	SOT313-2

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BLOCK DIAGRAM

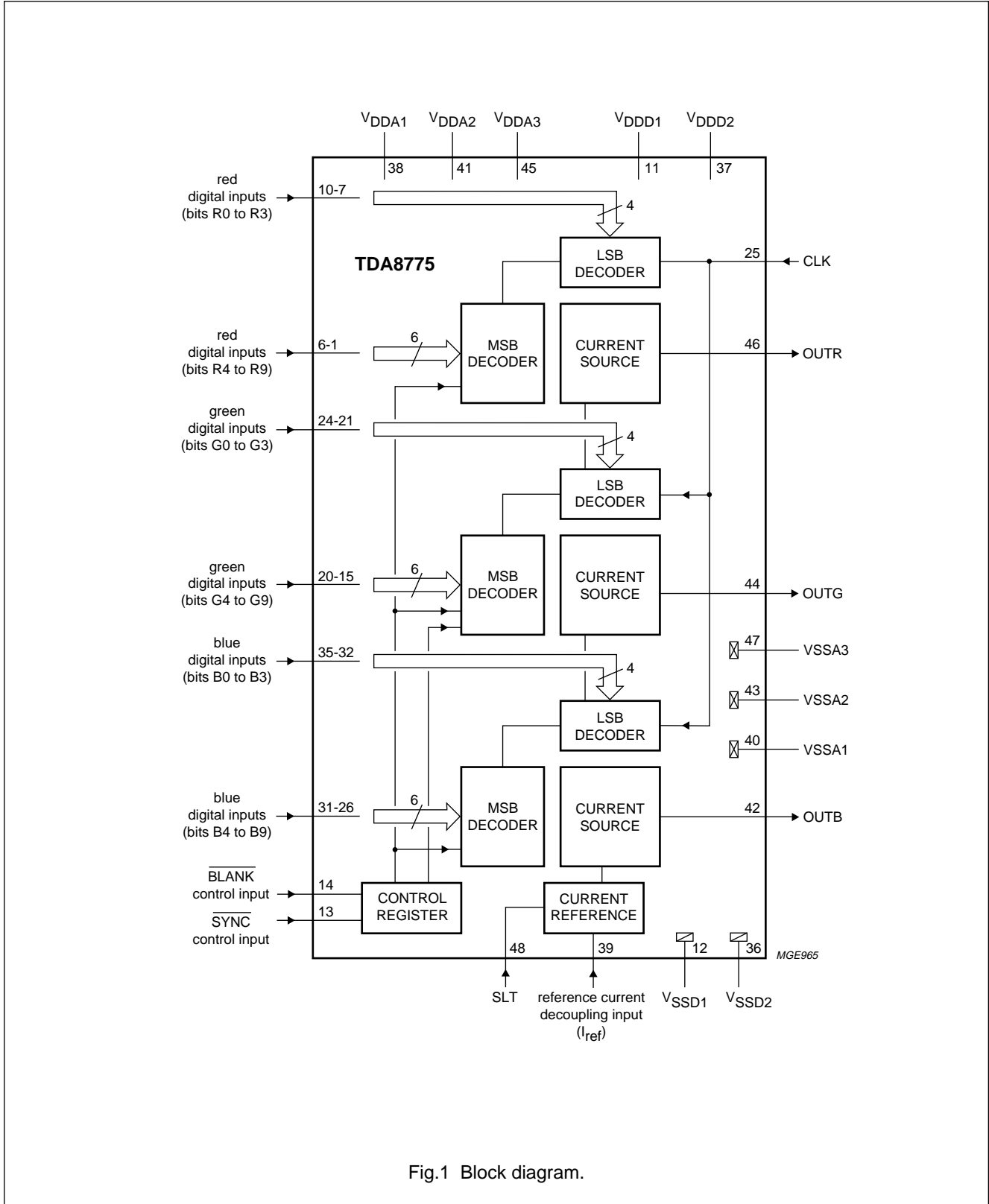


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
R9	1	red digital input data; bit 9 (MSB)
R8	2	red digital input data; bit 8
R7	3	red digital input data; bit 7
R6	4	red digital input data; bit 6
R5	5	red digital input data; bit 5
R4	6	red digital input data; bit 4
R3	7	red digital input data; bit 3
R2	8	red digital input data; bit 2
R1	9	red digital input data; bit 1
R0	10	red digital input data; bit 0 (LSB)
V _{DDD1}	11	digital supply voltage 1
V _{SSD1}	12	digital supply ground 1
$\overline{\text{SYNC}}$	13	composite sync control input; for green channel only (active LOW)
$\overline{\text{BLANK}}$	14	composite blank control input (active LOW)
G9	15	green digital input data; bit 9 (MSB)
G8	16	green digital input data; bit 8
G7	17	green digital input data; bit 7
G6	18	green digital input data; bit 6
G5	19	green digital input data; bit 5
G4	20	green digital input data; bit 4
G3	21	green digital input data; bit 3
G2	22	green digital input data; bit 2
G1	23	green digital input data; bit 1
G0	24	green digital input data; bit 0 (LSB)
CLK	25	clock input
B9	26	blue digital input data; bit 9 (MSB)
B8	27	blue digital input data; bit 8
B7	28	blue digital input data; bit 7
B6	29	blue digital input data; bit 6
B5	30	blue digital input data; bit 5
B4	31	blue digital input data; bit 4
B3	32	blue digital input data; bit 3
B2	33	blue digital input data; bit 2
B1	34	blue digital input data; bit 1
B0	35	blue digital input data; bit 0 (LSB)
V _{SSD2}	36	digital supply ground 2
V _{DDD2}	37	digital supply voltage 2
V _{DDA1}	38	analog supply voltage 1
I _{ref}	39	decoupling pin for reference current
V _{SSA1}	40	analog supply ground 1

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SYMBOL	PIN	DESCRIPTION
V _{DDA2}	41	analog supply voltage 2
OUTB	42	blue analog output
V _{SSA2}	43	analog supply ground 2
OUTG	44	green analog output
V _{DDA3}	45	analog supply voltage 3
OUTR	46	red analog output
V _{SSA3}	47	analog supply ground 3
SLT	48	mode selection; normal mode, R _L = 37.5 Ω (active HIGH); low power mode, R _L = 150 Ω (active LOW)

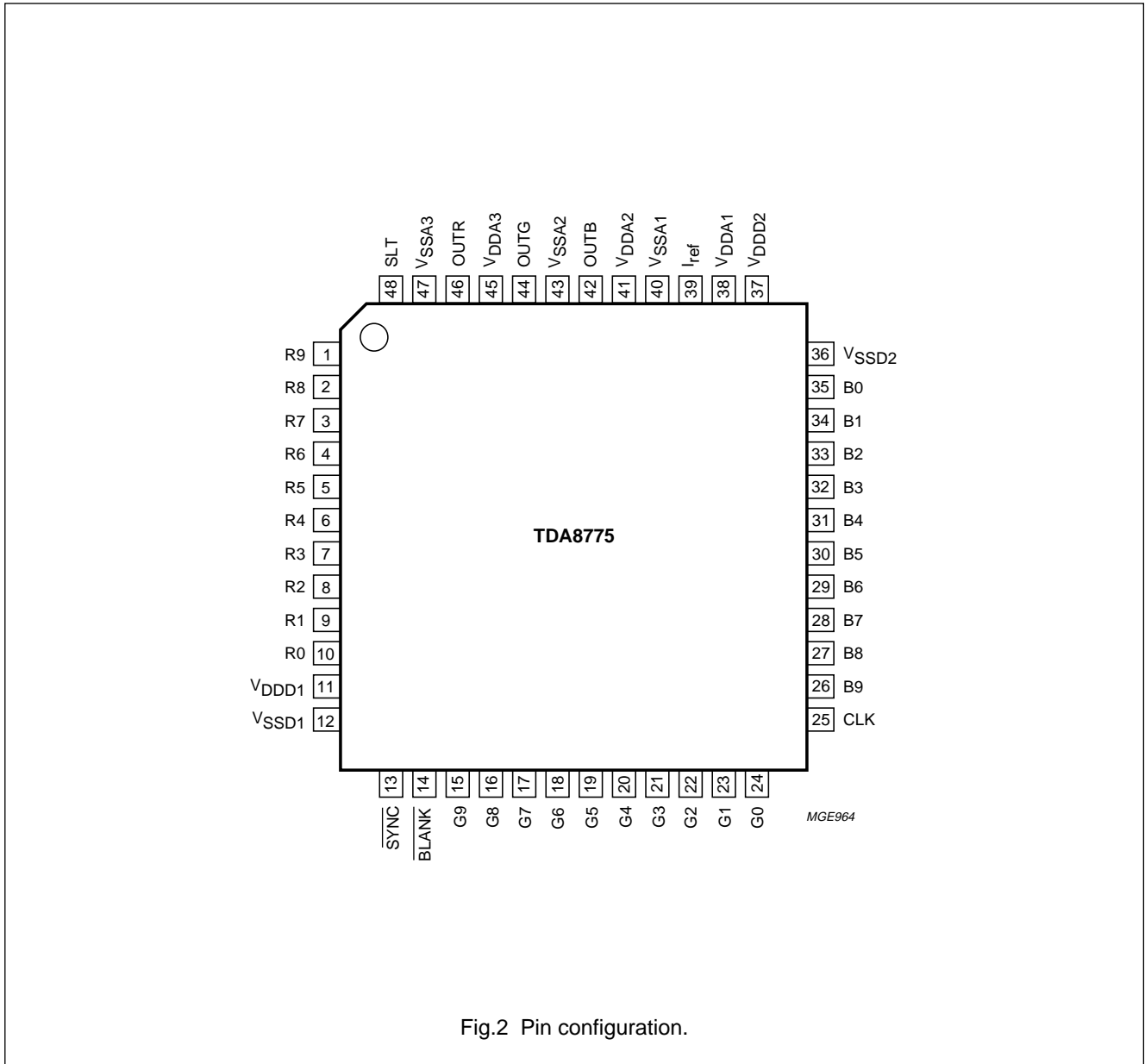


Fig.2 Pin configuration.

Triple 10-bit video Digital-to-Analog Converter (DAC)

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	-0.5	+6.5	V
V_{DDD}	digital supply voltage	-0.5	+6.5	V
ΔV_{DD}	supply voltage difference between V_{DDA} and V_{DDD}	-1.0	+1.0	V
T_{stg}	storage temperature	-55	+150	°C
T_{amb}	operating ambient temperature	0	70	°C
T_j	junction temperature	-	125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE (TYP.)	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	72	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

TDA8775 operating at 50 MHz; SLT = 1 and $R_L = 37.5\ \Omega$.

$V_{DDA} = V_{DDD} = 4.5$ to 5.5 V; V_{SSA} and V_{SSD} shorted together; $V_{DDA} - V_{DDD} = -0.5$ to $+0.5$ V; $T_{amb} = 0$ to $+70$ °C; typical values measured at $V_{DDA} = V_{DDD} = 5$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	SLT = 1; $R_L = 37.5\ \Omega$	-	67	tbf	mA
		SLT = 0; $R_L = 150\ \Omega$	-	16	tbf	mA
I_{DDD}	digital supply current	SLT = 1; $R_L = 37.5\ \Omega$	-	15	tbf	mA
		SLT = 0; $R_L = 150\ \Omega$	-	10	tbf	mA
Inputs						
CLOCK INPUT (PIN 25)						
V_{IL}	LOW level input voltage		$V_{SSD} - 0.5$	-	0.8	V
V_{IH}	HIGH level input voltage		2.0	-	$V_{DDD} + 0.5$	V
BLANK AND SYNC INPUTS (PINS 13 AND 14; ACTIVE LOW)						
V_{IL}	LOW level input voltage		$V_{SSD} - 0.5$	-	0.8	V
V_{IH}	HIGH level input voltage		2.0	-	$V_{DDD} + 0.5$	V
R, G AND B DIGITAL INPUTS (PINS 1 TO 10, 15 TO 24 AND 26 TO 35)						
V_{IL}	LOW level input voltage		$V_{SSD} - 0.5$	-	0.8	V
V_{IH}	HIGH level input voltage		2.0	-	$V_{DDD} + 0.5$	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing ($C_L = 25$ pF); see Fig.4						
$f_{clk(max)}$	maximum clock frequency	SLT = 1; $R_L = 37.5 \Omega$	50	–	–	MHz
		SLT = 0; $R_L = 150 \Omega$	35	–	–	MHz
t_{CPH}	clock pulse width HIGH		6	–	–	ns
t_{CPL}	clock pulse width LOW		6	–	–	ns
t_r	clock rise time		–	–	4	ns
t_f	clock fall time		–	–	4	ns
$t_{SU;DAT}$	input data set-up time		4	–	–	ns
$t_{HD;DAT}$	input data hold time		2.5	–	–	ns
Outputs						
OUTB, OUTR AND OUTG ANALOG OUTPUTS (PINS 42, 46 AND 44, REFERENCED TO V_{SSA}) FOR 37.5Ω LOAD						
V_{OUTmax}	maximum output voltage	BLANK and SYNC active				
		R and B channels	–	0.714	–	V
		G channel	–	1.0	–	V
THD	total harmonic distortion	$f_i = 4.43$ MHz; SLT = 1; $f_{clk} = 50$ MHz; $R_L = 37.5 \Omega$	–	–52	–	dB
		$f_i = 4.43$ MHz; SLT = 0; $f_{clk} = 35$ MHz; $R_L = 150 \Omega$	–	–50	–	dB
Z_L	output load impedance	SLT = 1	tbf	37.5	tbf	Ω
		SLT = 0	tbf	150	tbf	Ω
Transfer function						
INL	DC integral non-linearity		–	± 1	± 2	LSB
DNL	DC differential non-linearity		–	± 0.7	± 1.0	LSB
α_{ct}	crosstalk DAC to DAC		tbf	–	–	dB
	DAC to DAC matching		–	1.0	tbf	%
Switching characteristics; see Fig.5						
t_d	input to 50% output delay time	full-scale change; SLT = 1; $R_L = 37.5 \Omega$	–	tbf	–	ns
		full-scale change; SLT = 0; $R_L = 150 \Omega$	–	tbf	–	ns
t_{s1}	settling time	10 to 90% full-scale change; SLT = 1; $R_L = 37.5 \Omega$	–	4	–	ns
		10 to 90% full-scale change; SLT = 0; $R_L = 150 \Omega$	–	10	–	ns
t_{s2}	settling time	to ± 1 LSB; SLT = 1; $R_L = 37.5 \Omega$	–	tbf	–	ns
		to ± 1 LSB; SLT = 0; $R_L = 150 \Omega$	–	tbf	–	ns
Output transients (glitches)						
V_g	area for 1 LSB change		–	tbf	–	LSB.ns

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Table 1 Input coding and DAC output currents (typical values)

BINARY INPUT				DAC OUTPUT CURRENT (mA)		DAC OUTPUT CURRENT (mA)	
				SLT = 1; R _L = 37.5 Ω		SLT = 0; R _L = 150 Ω	
SYNC	BLANK	DATA	CODE	R, B Channels	G Channel	R, B Channels	G Channel
0	0	XXH	–	0	0	0	0
1	0	XXH	–	0	7.62	0	1.90
0	1	00H	0	1.44	1.44	0.36	0.36
		–	–	–	–	–	–
		3FFH	1023	19.05	19.05	4.76	4.76
1	1	00H	0	1.44	9.05	0.36	2.26
		–	–	–	–	–	–
		3FFH	1023	19.05	26.67	4.76	6.67

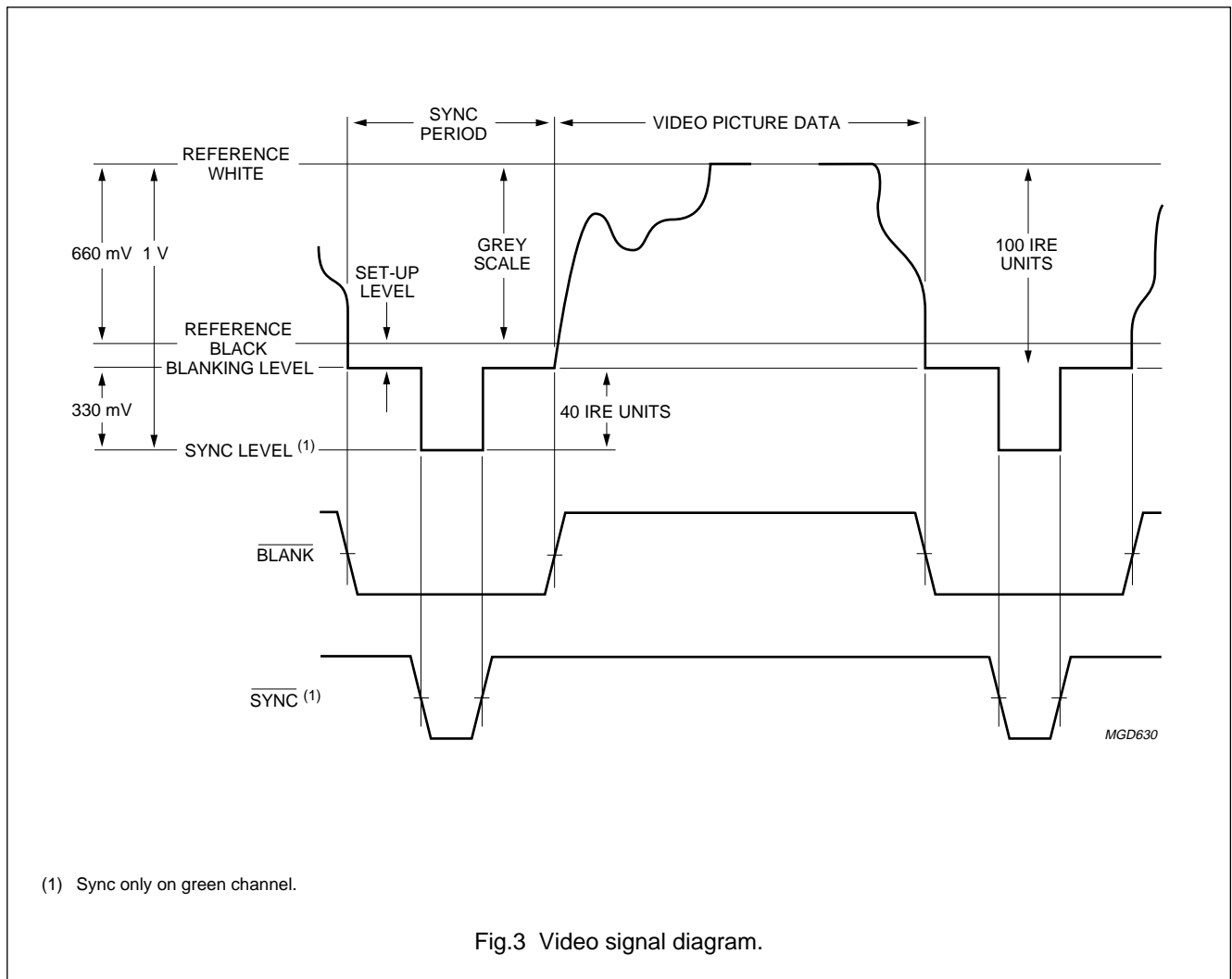


Fig.3 Video signal diagram.

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TIMING

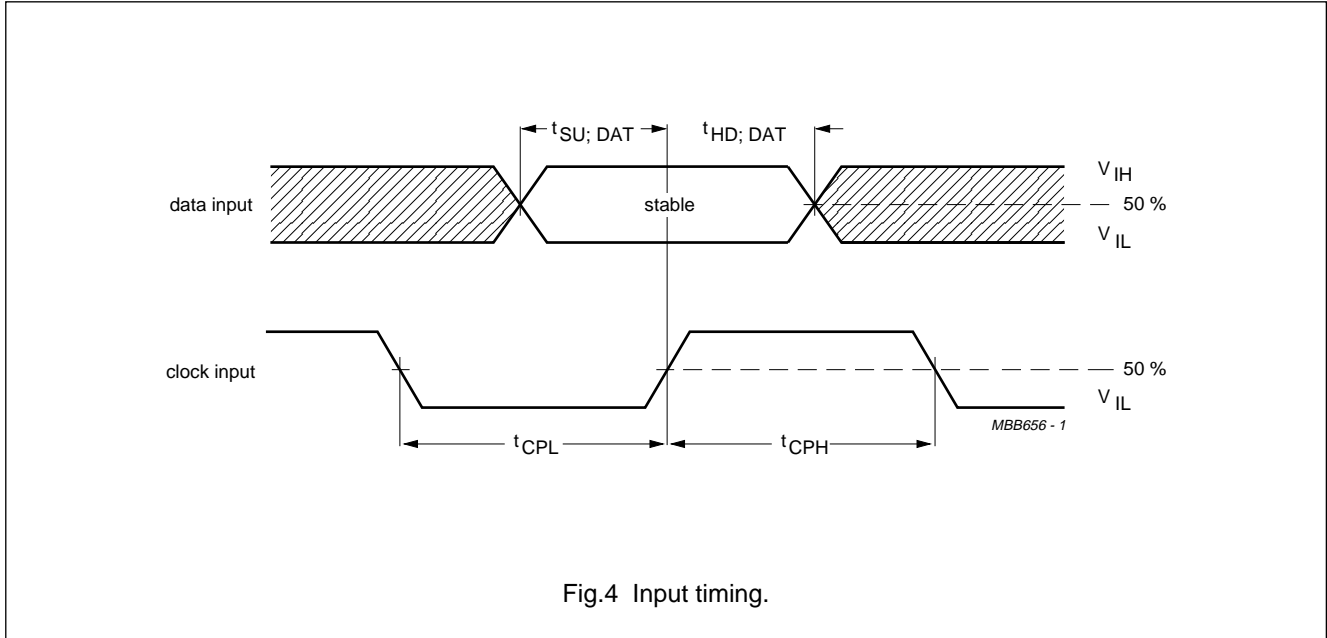
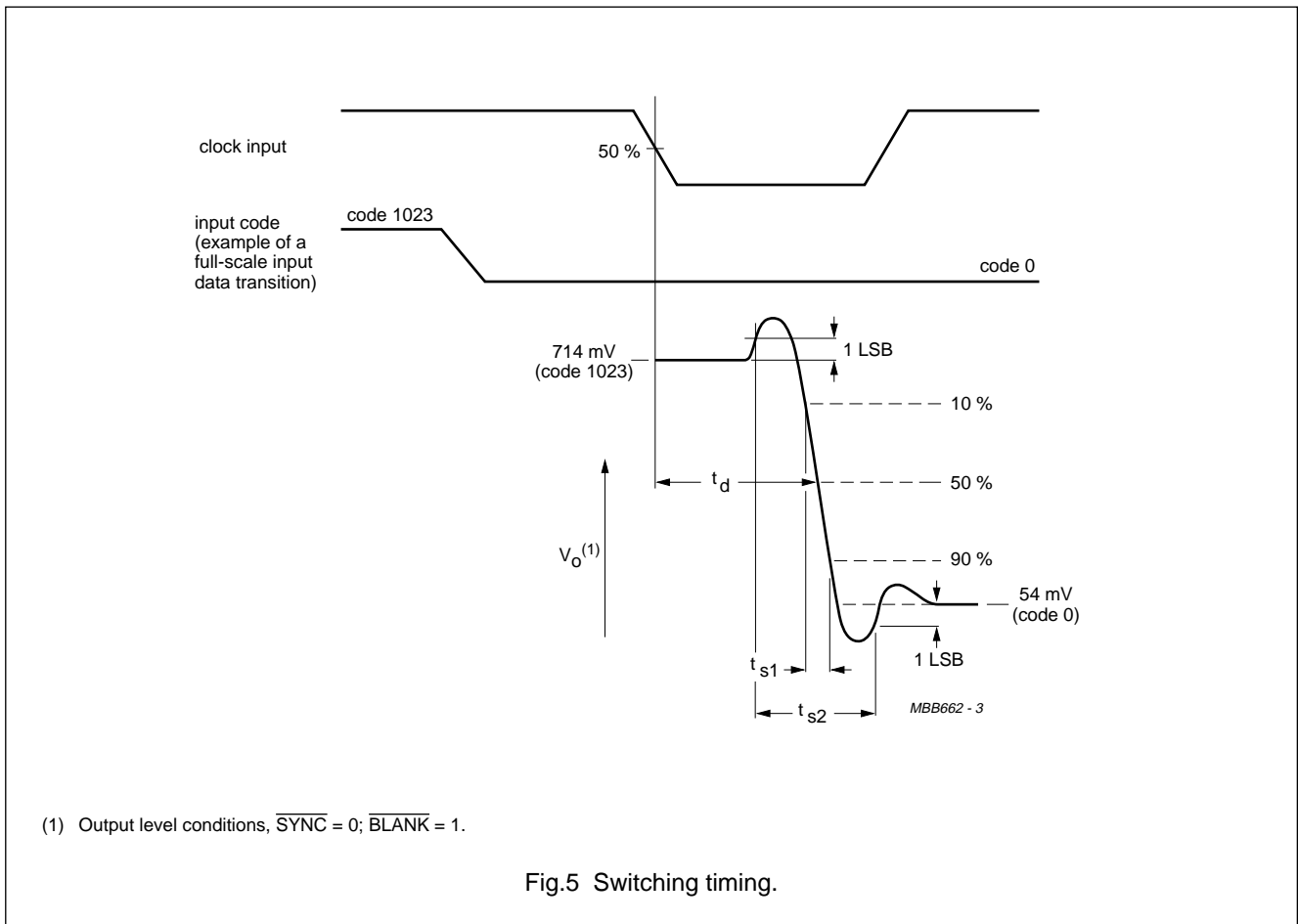


Fig.4 Input timing.



(1) Output level conditions, $\overline{SYNC} = 0$; $\overline{BLANK} = 1$.

Fig.5 Switching timing.

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INTERNAL PIN CIRCUITRY

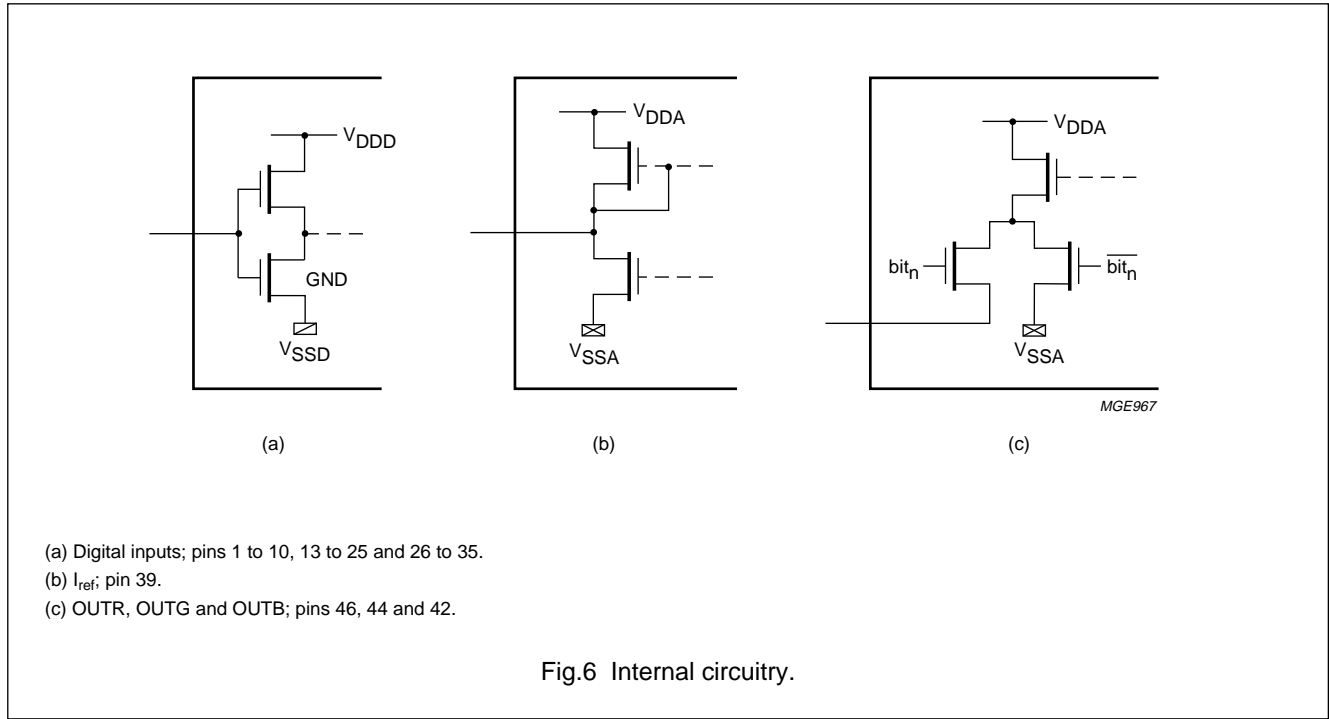
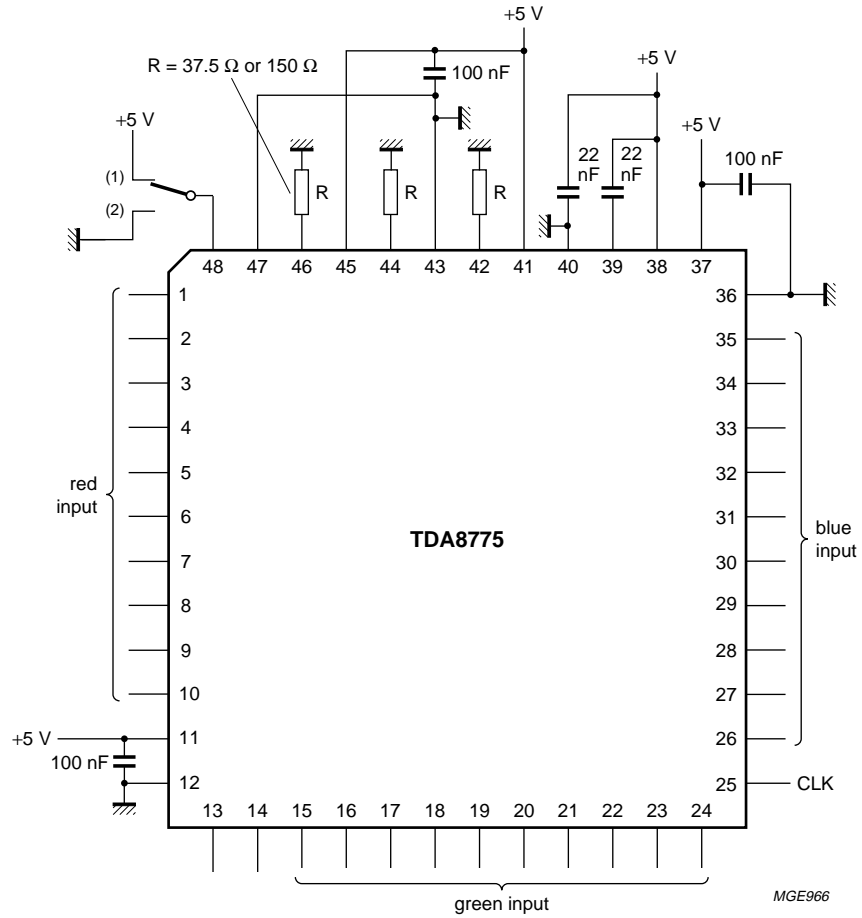


Fig.6 Internal circuitry.

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APPLICATION INFORMATION



Analog and digital supplies should be separated and decoupled.
 Supplies are not connected internally.
 All ground pins must be connected. One ground plane is preferred although it depends on the application.
 (1) R = 37.5 Ω ; SLT = 1.
 (2) R = 150 Ω ; SLT = 0.

Fig.7 Application diagram.

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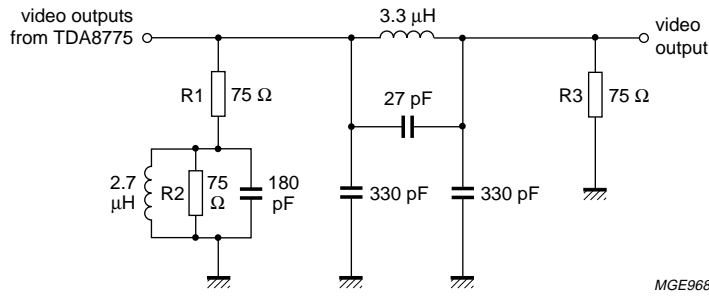


Fig.8 Example of reconstruction filter for 1 V output swing.

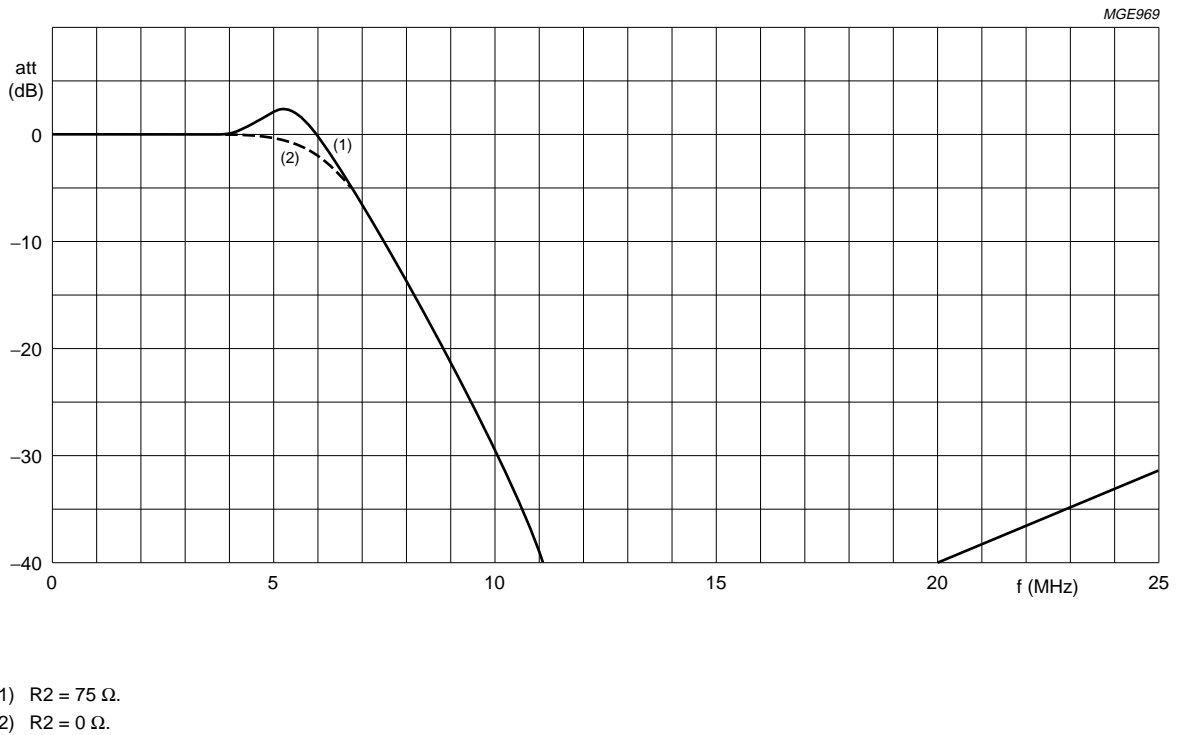


Fig.9 Frequency response for filter shown in Fig.8.

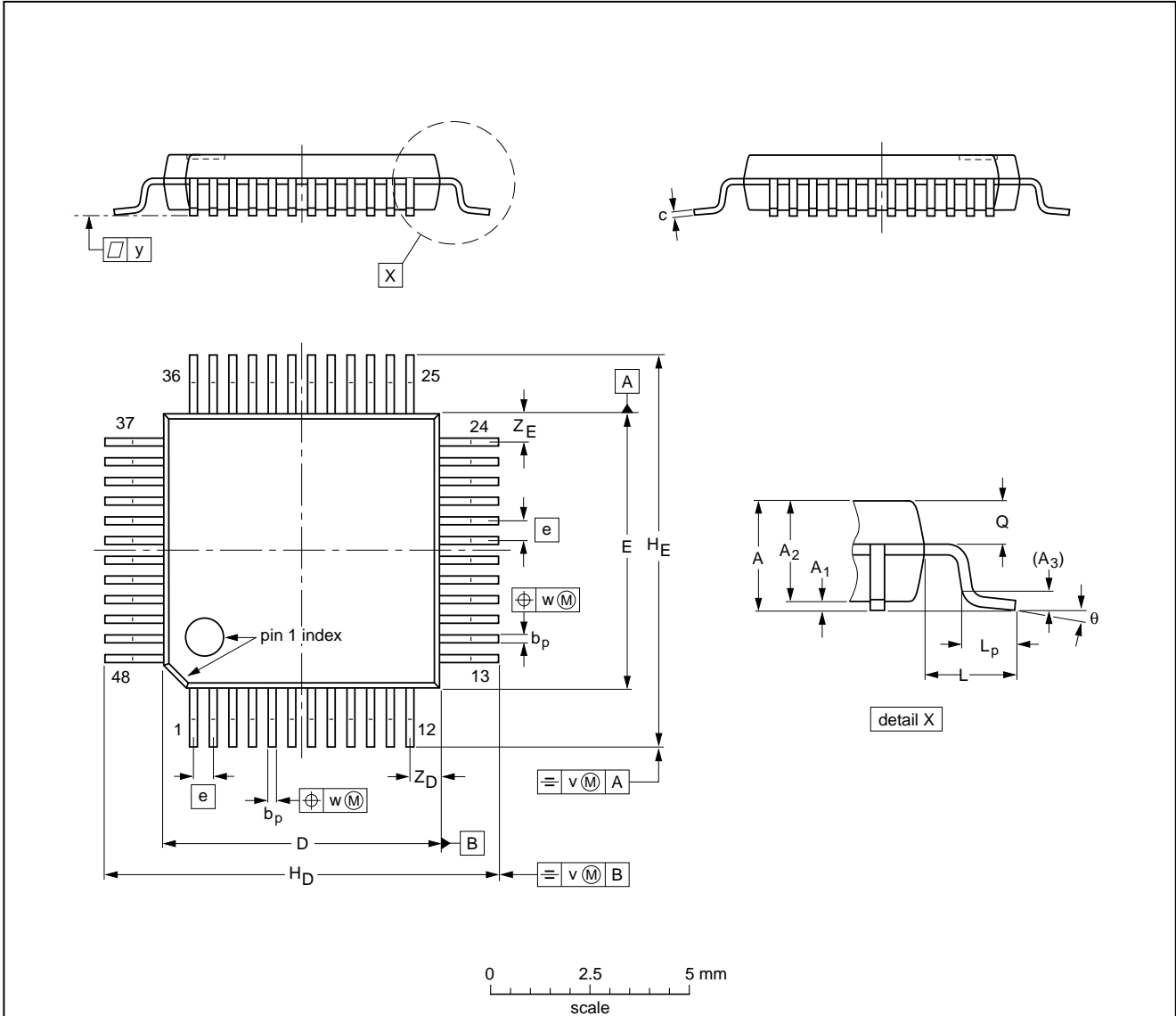
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PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

SOT313-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	Q	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						93-06-15 94-12-19

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "*IC Package Databook*" (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113, Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor, 51 James Bourchier Blvd., 1407 SOFIA, Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 615 800, Fax. +358 615 80920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex, Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS, Tel. +30 1 4894 339/911, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd. Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3, 20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 926 5361, Fax. +7 095 564 8323

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale, 2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000, Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51, 04552-903 São Paulo, SÃO PAULO - SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA, Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66, Chung Hsiao West Road, Sec. 1, P.O. Box 22978, TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd., 209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260, Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL, Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7, 252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381

Uruguay: see South America

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